Attached Scanned PDF

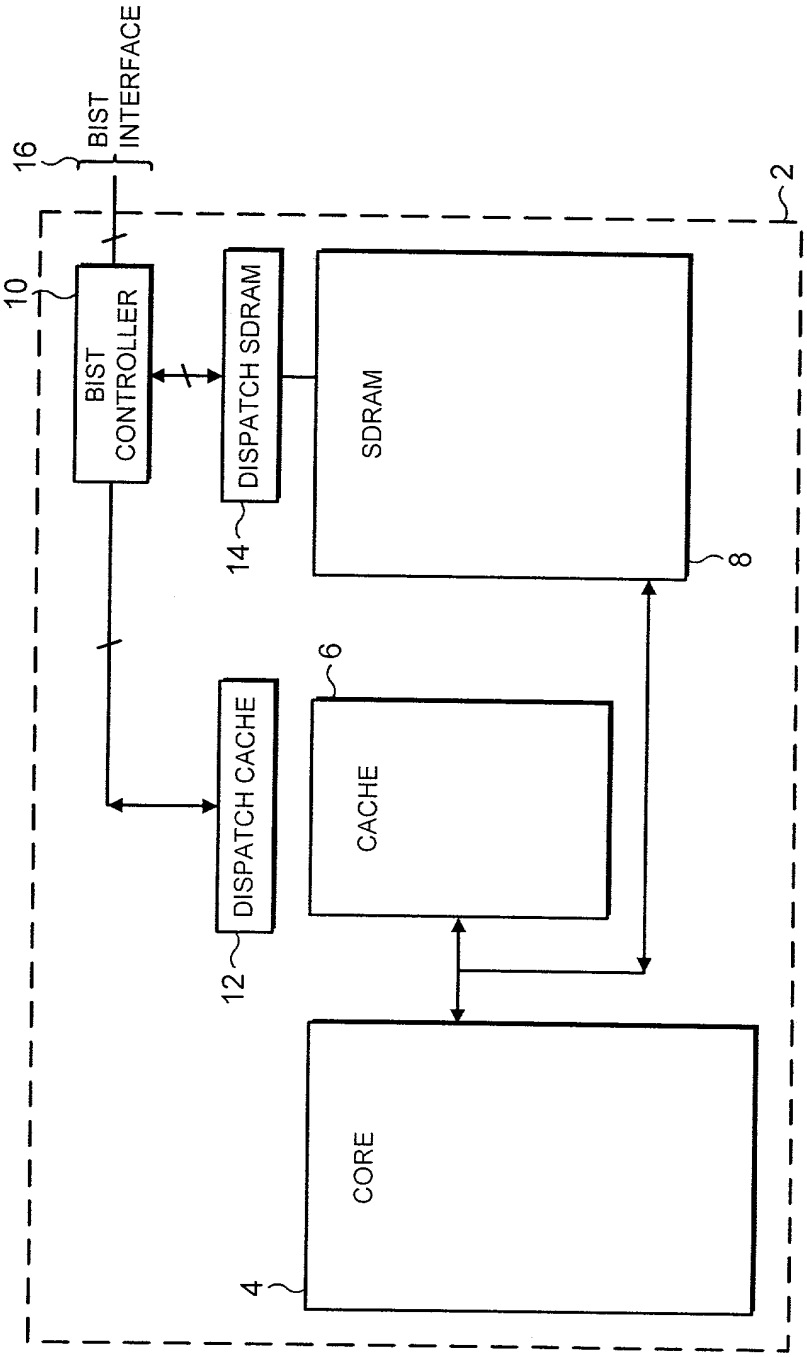

FIG. 1

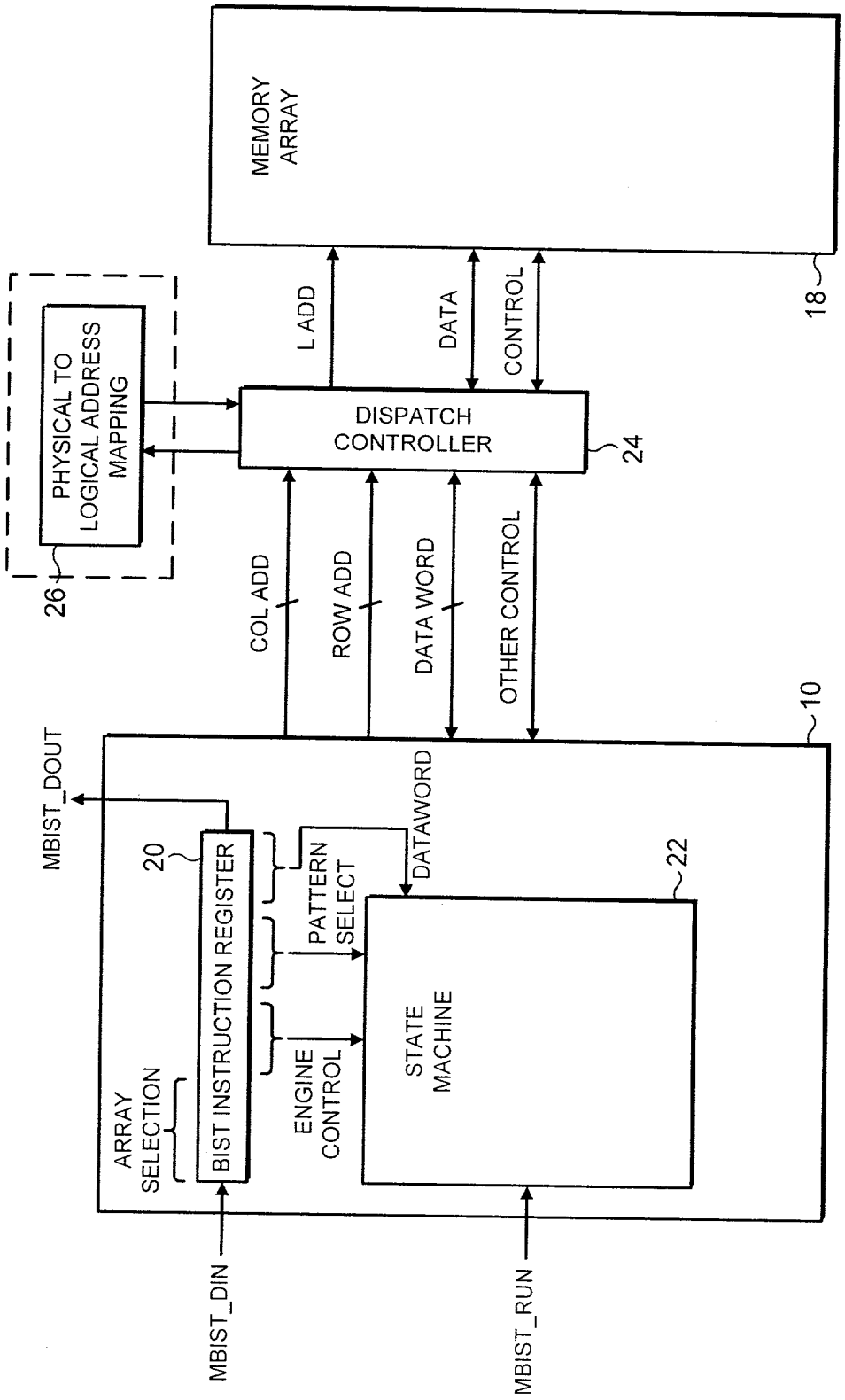
MEMORY ARRAY
18
L ADD
DATA
CONTROL
PHYSICAL TO LOGICAL ADDRESS MAPPING
26
DISPATCH CONTROLLER
24
COL ADD
ROW ADD
DATA WORD
OTHER CONTROL
10
MBIST_DOUT
20
BIST INSTRUCTION REGISTER
ARRAY SELECTION
ENGINE CONTROL
PATTERN SELECT
DATAWORD
22
STATE MACHINE
MBIST_DIN
MBIST_RUN

FIG. 2

Appendix - Drawings

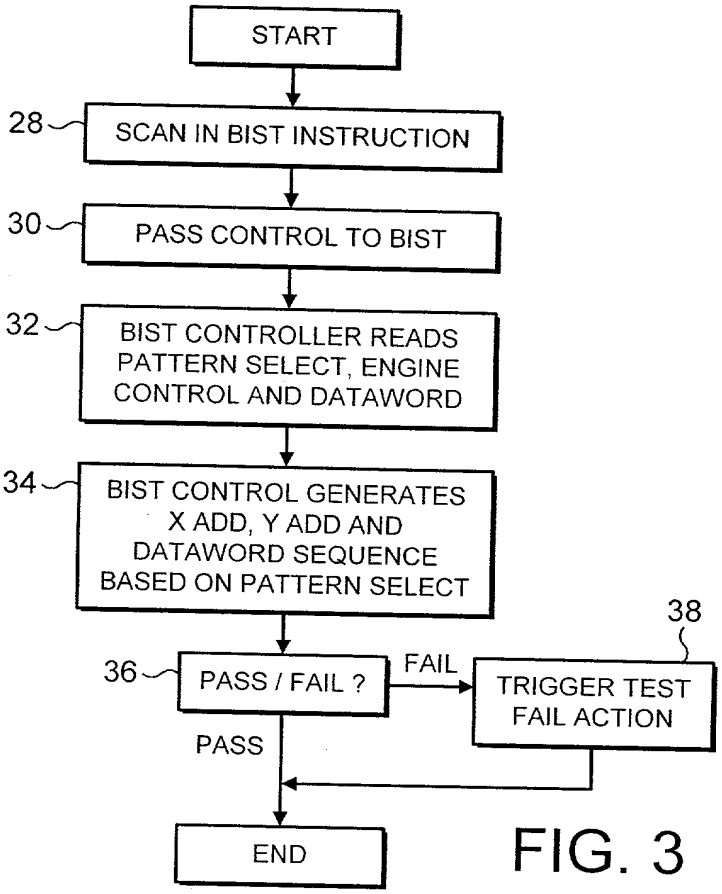

FIG. 3

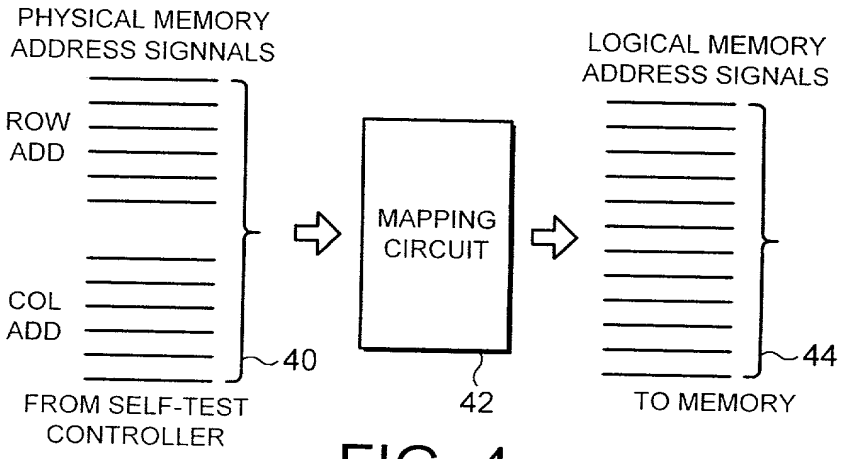

FIG. 4

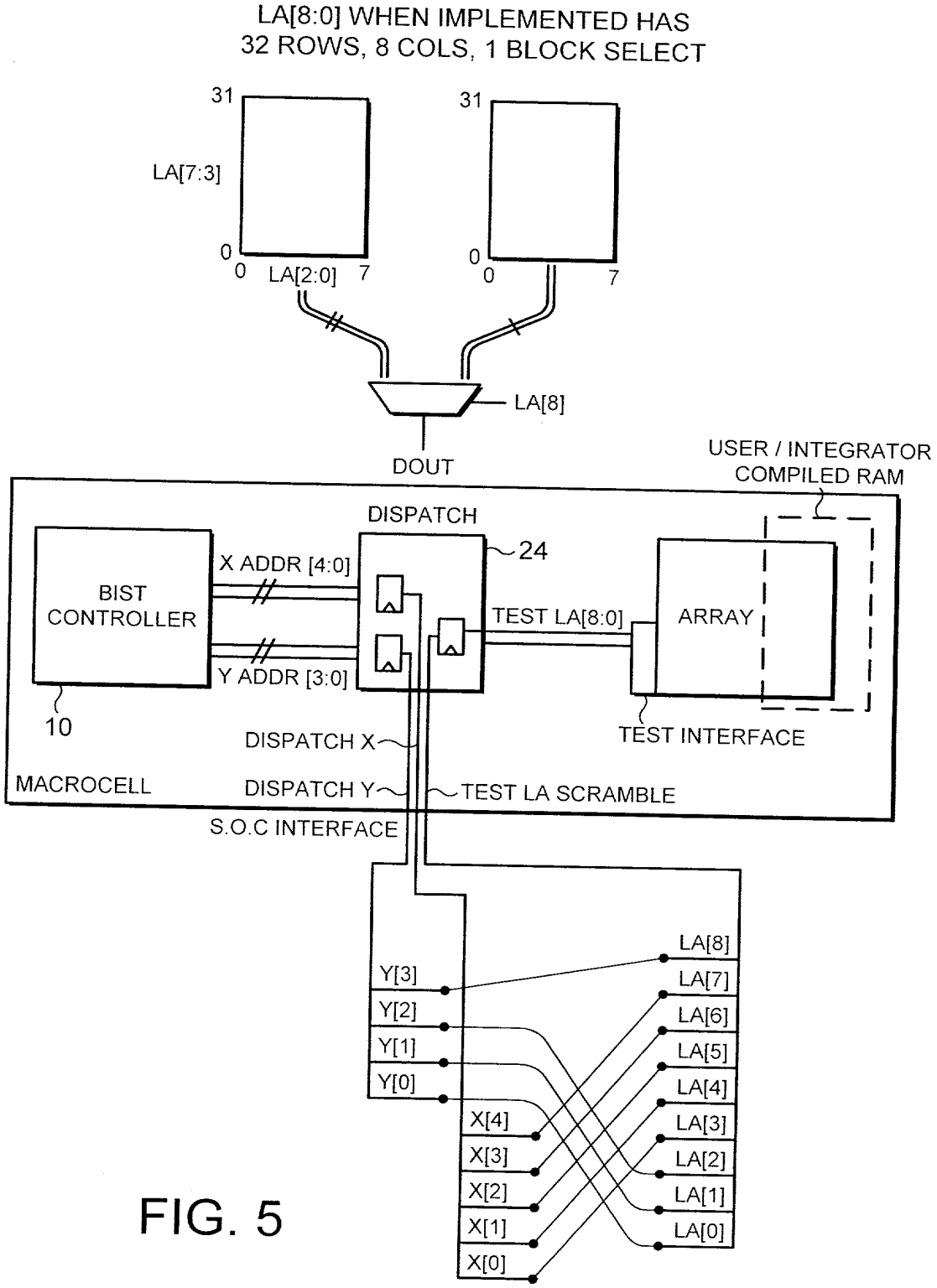
LA[8:0] WHEN IMPLEMENTED HAS
32 ROWS, 8 COLS, 1 BLOCK SELECT
31
LA[7:3]
0
0
LA[2:0]
7
31
0
0
7
LA[8]
DOUT
USER / INTEGRATOR
COMPILED RAM
DISPATCH
24
BIST
CONTROLLER
X ADDR [4:0]
Y ADDR [3:0]
TEST LA[8:0]
ARRAY
10
TEST INTERFACE
DISPATCH X
MACROCELL
DISPATCH Y
TEST LA SCRAMBLE
S.O.C INTERFACE
Y[3]
Y[2]
Y[1]
Y[0]
X[4]
X[3]
X[2]
X[1]
X[0]
LA[8]
LA[7]
LA[6]
LA[5]
LA[4]
LA[3]
LA[2]
LA[1]
LA[0]

FIG. 5